A CMOS Fifth-Order 400MHz Current-Mode LF Linear Phase Filter for Hard Disk Read Channels

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Abstract—**A 400MHz CMOS fifth-order linear phase g_m-c filter based on current-mode (CM) leapfrog (LF) structure is realized. The filter is implemented using a fully-differential linear operational transconductance amplifier (OTA) based on source degeneration topology. PSpice simulations in a standard TSMC 0.18μm CMOS process and with 2.5V power supply have shown that the cut-off frequency of the filter ranges from 330MHz to 450MHz and dynamic range is about 64dB. The group delay is approximately 4% over the whole tuning range and total power consumption is only 190mW at 400MHz cut-off frequency.**

I. Introduction

The design of analogue circuits with high frequency operation and low power consumption has received world-wide attention for over 20 years. In recent years, several continuous-time integrated filters have been realized successfully and used for computer hard disk drive (HDD) design [1-7]. The HDD industry is looking for developments in read channel chips to push data rates to a higher speed, along with low power and low cost solutions. However, designing filters operating at UHF in pure CMOS process is a big challenge. The small-signal transconductance of CMOS devices, unlike bipolar devices, increases with both current and gate dimensions, and usually for high-frequency applications the resulting circuits require high power consumption and huge transistor dimensions that increase the parasitic capacitance.

Continuous-time filter design using cascade and LC ladder simulation methods have been developed very well. However, results have shown that cascade structures possess higher magnitude sensitivity; filters based on LC ladder simulation cannot realize real zeros directly, since LC ladder prototypes can only produce imaginary zeros. Therefore, multiple loop feedback (MLF) structures have been introduced for HDD read channel filtering. On the other hand, analog signal processing in current domain can offer advantages for many applications and current-mode (CM) filters have received much attention. For current signal processing and filtering, circuits are normally based on current integrators, current amplifiers, and current feedback, with current inputs to circuit nodes and current outputs from OTA output terminals. In this paper a fifth-order linear phase low-pass filter with gain boost using current-mode MLF LF structure is described.

The paper is organized in five sections. The filter architecture and synthesis are described in Section II. The design of a fully-balanced two inputs and four outputs OTA is discussed in Section III. The simulation results are given in Section IV, and finally conclusions are given in Section V.

II. Filter Architecture and Synthesis

The 7th order linear phase filter was used in the literature [4-6]. In this paper, we propose a 5th order current-mode LF linear phase filter for computer HDD read channels. A critical design aspect of filters performing the equalization function is the gain boost capability. Boosting is done to shape the spectrum of the received signal according to the desired equalization of a PRML read channel. This feature is typically realized through two real zeroes without changing the group delay response. Several topologies have been proposed to realize these symmetric zeros. Many of them make use of additional circuits (amplifiers, derivators, etc.) that require a large amount of power to keep the parasitic poles out of the band of interest. In the circuit shown in Figure 1, the zeros are realized by just adding two extra OTAs.

The normalized characteristic of a fifth-order lowpass equiripple linear phase filter with real zeros at the cut-off frequency is given by:

$$H_d(s) = \frac{(s^2 - 1)}{d(s)} \qquad (1)$$

With

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$$d(s) = 0.201926s^5 + 0.822285s^4 + 2.075924s^3 + 3.033116s^2 + 2.604527s + 1$$

The fully-balanced OTA-C realization of the function in (1) using the CM LF structure with output summation OTAs is shown in Figure 1. With $\tau_j = C_j/g_j$, $\alpha_j = g_{aj}/g_j$ the overall transfer function of the circuit can be derived as:

$$H(s) = \frac{I_{out(GB)}}{I_{in}} = \frac{N(s)}{D(s)} \quad (2)$$

Where

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5 s^5 + \tau_2\tau_3\tau_4\tau_5 s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_4\tau_5 + \tau_3\tau_4\tau_5)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_4\tau_5)s^2 + (\tau_1 + \tau_3 + \tau_5)s + 1$$

$$N(s) = \alpha_3\tau_4\tau_5 s^2 + (\alpha_3 + \alpha_5)$$

The design formulae for the equalizer can be attained by coefficient matching between (1) and (2) [8, 9]. The resulting pole and zero parameters are:

$$\tau_1 = 0.24557, \tau_2 = 0.61776, \tau_3 = 0.84468, \tau_4 = 1.04066,$$
$$\tau_5 = 1.51427, \alpha_3 = 0.36544, \alpha_5 = 0.63456$$

The equalizer is designed with identical unit OTAs using the CMOS OTA cell in Figure 2, with selected transconductance g_j of 1.6mS, to improve OTA matching and facilitate design automation. The design of the unity OTA will be discussed in next section. The cut-off frequency of the equalizer is chosen as 400 MHz. Using the computed parameter values, the capacitor values can be calculated, but the parasitic capacitance must also be taken into account. For the circuit of Figure 2, the parasitic capacitance is about 0.15pF. The capacitance values are recalculated below:

$$C_1 = C_6 = 0.1387\,pF, C_2 = C_7 = 0.6521\,pF,$$
$$C_3 = C_8 = 0.9651\,pF, C_4 = C_9 = 1.2355\,pF,$$
$$C_5 = C_{10} = 1.8887\,pF, g_{a3} = 585\mu S, g_{a5} = 1015\mu S$$

III. FULLY-BALANCED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Fast data transmission requires high performance filtering blocks, most of the cases with linear phase characteristics. OTA-C filters are an option for these applications provided that they are compliant with both linearity and frequency specifications. The OTA is one of the most important blocks for the UHF applications. Topologies based on pseudo-differential pair amplifiers have been used in [10]. This approach can be very efficient in terms of power consumption but the rejection to supply noise is limited, especially for high frequency circuits. The tunable OTA based on input differential pair with source degeneration has been used for a long time [5-8, 11]. This technique improves linearity of the circuit by using local feedback; the larger the feedback (source degeneration factor) the better linearity is. Large transconductances are needed for the implementation of high-frequency filters. The implementation of large transconductances requires the use of wider and shorter transistors. However, the use of large transistor widths can cost more power and increase excess phase of the OTA at high frequency. The use of small transistor lengths pushes the parasitic poles to higher frequencies, but the OTA DC gain is reduced and mobility degradation effects become more severe.

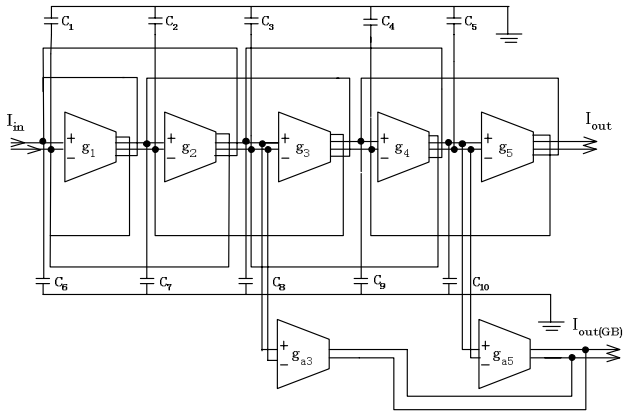

Figure 1 Fifth-order CM LF OTA-C equalizer with output summation OTAs

In order to match the structure of the filter which we presented in section II, the two input and four output OTA are needed. The proposed multiple input and multiple output OTA is presented in Figure 2, the sources of the input devices are connected to their substrate, which is a common P–well to prevent body effects.

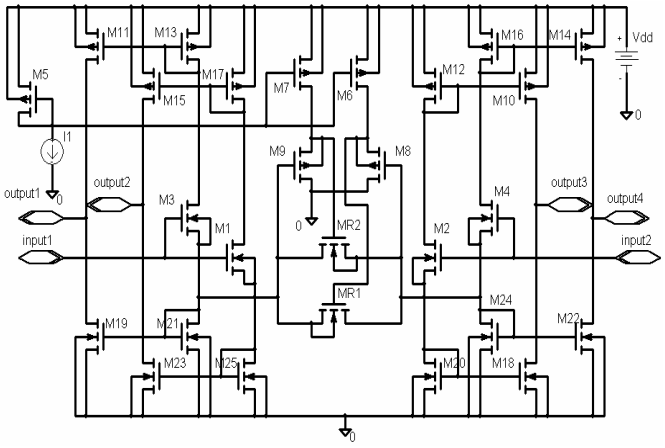

Figure 2 Fully-balanced OTA unit cell

The presented structure uses two parallel differential pairs in the input stage. The output stages consist of eight current mirrors. The input stage currents are differentially mirrored through P–type current mirrors $M_{10,12}$ $M_{11,13}$ $M_{14,16}$ $M_{15,17}$ and N–type current mirrors $M_{18,20}$ $M_{19,21}$ $M_{22,24}$ $M_{23,25}$ to the outputs. Assuming matching between transistors, the output differential current $I_{out} = I_{output1} - I_{output4} = I_{output2} - I_{output3}$. The gate voltages of M_{R1} and M_{R2}

are connected to the separate source followers M_9 and M_8 biased with a control current I_1, so that both DC level shifts are identical and tuning is obtained via I_1 without disturbing the bias current of the input stage. It is worth mentioning that the geometry of the input devices also affects the DC transconductance value, and these are usually designed to be large in order to improve matching of threshold voltage V_T and K between the transconductance stages. In order to shift the poles to higher frequencies and get the large transconductance the channel length used for these devices is the minimum length allowed by the process. The M_{R1} and M_{R2} are connected in parallel to increase the total transconductance value and therefore the widths of four input stage transistors can be designed quite small, which can optimize the power consumption, parasitic effects and high frequency response. Using a first-order transistor model and neglecting the mobility degradation and output resistance effects, we have:

$$I_D = \frac{(V_{cm} - 2V_T)^2}{2 \cdot (\sqrt{\frac{L_1}{\mu_n C_{OX} W_1}} + \sqrt{\frac{L_2}{\mu_n C_{OX} W_2}})^2} \tag{3}$$

Where I_D is the drain current of transistors of M_1 and M_2, V_{cm} is the supplied common mode voltage. V_T is the threshold voltage. L_1, W_1, L_2, W_2 are the width and length of transistors M_1 and M_2, respectively and μ_n, and C_{ox}, are mobility, and oxide capacitance per unit area. Therefore, the transconductance of M_1 and M_2 are expressed as:

$$\begin{aligned} g_{m1} &= \sqrt{2\mu_n C_{OX} \frac{W_1}{L_1} I_D} \\ g_{m2} &= \sqrt{2\mu_n C_{OX} \frac{W_2}{L_2} I_D} \end{aligned} \tag{4}$$

The total transconductance of the proposed OTA can be expressed as (g_{m1}=g_{m2}):

$$g_m = \frac{g_{m1}}{g_{m1} \cdot R + 1} \tag{5}$$

The source degeneration factor is defined as $N=g_{m1}R$, R is the resistance of the source degeneration transistors.

The differential pair formed by M_1, M_2 is degenerated by two NMOS transistors operating in triode region (M_{R1}, M_{R2}). The total drain current of MOS transistors M_{R1} and M_{R2} in triode region is given by, where V_{ds} is much smaller than V_{GS}-V_T

$$I_{R1,2} = 2K(V_{GS} - V_T)V_{ds} \tag{6}$$

Where $K=0.5\mu_n C_{ox}(W/L)$ is the N–type transconductance parameter. Then:

$$I_{out} = I_{R1,2} - (-I_{R1,2}) = 2I_{R1,2} \tag{7}$$

By substituting (6) into (7) we get:

$$I_{out} = 4K(V_{GS} - V_T)V_{ds} \tag{8}$$

Note that $V_{ds} \approx V_{id}$ when source degeneration is deep. Therefore, we get:

$$I_{out} \approx 4K(V_{GS} - V_T)V_{id} = \frac{V_{id}}{R} = g_m \cdot V_{id} \tag{9}$$

Where $V_{id} = V_{input1} - V_{input2,}$ V_{id} is the differential input voltage and g_m is the DC transconductance of the OTA given by:

$$g_m = \frac{1}{R} = 4K \cdot V_B, V_B = V_{GS} - V_T \tag{10}$$

From (9) and (10), we can see that the OTA exhibits a linear V–I characteristic with the assumptions made. However, in practice, second–order effects such as body effects, mobility reduction, and channel length modulation will degrade the V–I function of the OTA. Equation (10) shows that the transconductance value can be controlled by varying the bias voltage V_B. Thus, the allowed values of V_B determine the achievable transconductance tuning range. As can be seen from the OTA circuit, tuning is performed by a loop controlling current I_1.

IV. SIMULATION RESULTS

The filter was designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18µm CMOS process available from MOSIS [12]. Figure 3 shows the magnitude response of the filter with and without the gain boost. As can be seen from Figure 3, the gain boost of the filter is about 6dB. By varying the bias current I_1 of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 330-450 MHz, as shown in Figure 4.

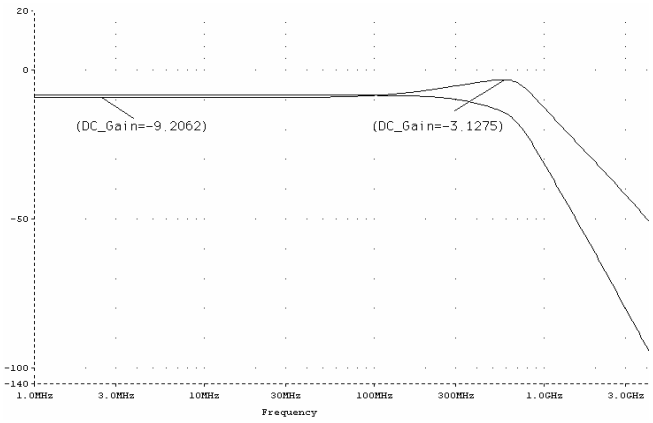

Figure 3 Simulated magnitude response of the filter without and with gain boost

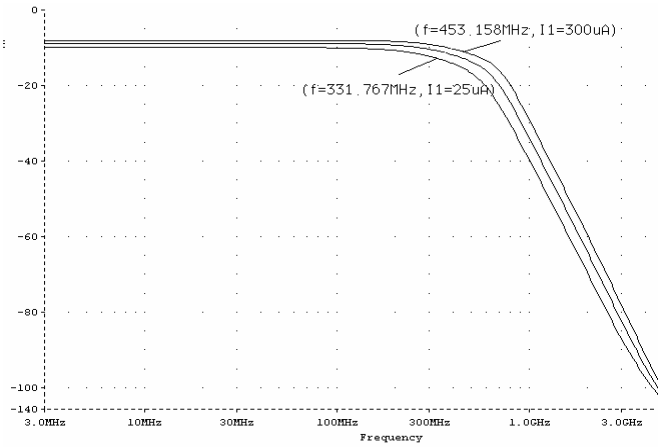

Figure 4 Simulated magnitude response of the filter with different bias currents

The filter phase response is fairly linear, as can be seen from Figure 5; the filter group delay ripple (GDR) up to twice of the cut-off frequency is approximately 4%. As can also be seen from Figure 5, the GDR of the filter with gain boost is only slightly different from the GDR of the filter without gain boost, which means the presented filter is very suitable for HDD read channels.

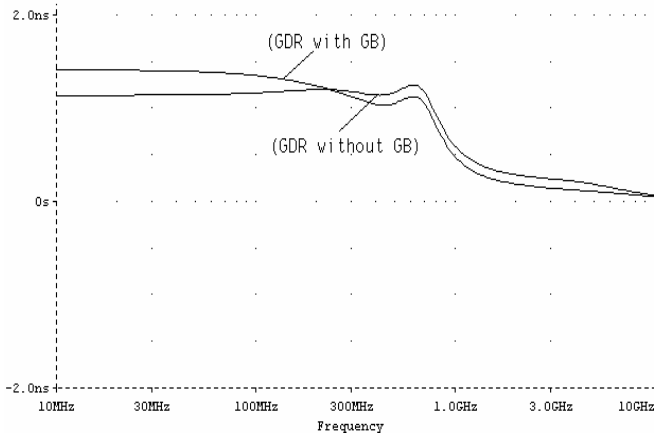

Figure 5 Simulated group delay response at f_c=400MHz

Simulations of the filter have shown a total harmonic distortion (THD) of less than 1% with a single tone of 1250µA at 10MHz. The dynamic range (DR) is over 64dB at f_c=400MHz and the total power consumption of the filter is about 190mW at 400MHz cut-off frequency for a single 2.5V power supply. The comparison of this circuit with some others in the literature is given in Table 1.

V. CONCLUSIONS

A CMOS 400MHz current-mode fifth-order linear phase leapfrog equalizer has been described. A linear multiple output OTA based on source degeneration topology with a typically large transconductance has been used. Simulation results in 2.5V 0.18µm CMOS have shown the frequency range of 330–450MHz, dynamic range of 64dB, power consumption of 190mW, and group delay ripple of 4%. These results have demonstrated that the proposed CM LF equalizer is well suitable for advanced hard disk read channel applications.

Table 1 COMPARISON WITH OTHER FILTER DESIGNS

Parameters	Specifications				
Reference	[1]	[3]	[4]	[5]	This work
Filter_Conf.	Cascade	VM LF	VM LF	CM LF	CM LF
Range MHz	30-120	8-32	50-150	150-250	330-450
GDR	3%	7%	4.50%	4.50%	4%
DR	45dB	55dB	65dB	66dB	64dB
PC mW	120	322	216	210	190
P. Supply	2.5V	5V	2.5V	2.5V	2.5V
CMOS Tech.	0.25um	0.25um	0.25um	0.18um	0.18um

GDR = group delay ripple; DR = dynamic range; PC = power consumption
VM = voltage–mode; CM = current–mode

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